Please replace the paragraph beginning at page 17, line 17, with the following rewritten paragraph. Per 37 C.F.R. § 1.121, this paragraph is also shown in Appendix A with notations to indicate the changes made.

The figures provide further information about the methods of the invention. Figure 1A illustrates one portion of a wafer 10 prior to planarization in accordance with the present invention having features that are filled with the material to be removed through planarization. The wafer portion 10 includes a substrate assembly 12 having junctions 16 formed thereon. A capacitor and/or barrier layer material 19 is then formed over the substrate assembly 12 and the junctions 16. The capacitor and/or barrier layer material 19 may be any conductive material such as platinum or any other suitable conductive second or third row Group VIII metal-containing capacitor and/or barrier material. Generally, as shown in Figure 1A, the nonplanar upper surface 13 of capacitor and/or barrier layer 19 is subjected to planarization or other processing in accordance with the present invention. The resulting wafer 10, which is shown in Figure 1B, includes an upper surface 17 planarized such that the thickness of the wafer 10 is substantially uniform across the entire wafer 10 so that the wafer now includes a capacitor and/or barrier structure layer 14.

Please replace the paragraph beginning at page 18, line 4, with the following rewritten paragraph. Per 37 C.F.R. § 1.121, this paragraph is also shown in Appendix A with notations to indicate the changes made.

Figure 2A illustrates one portion of a wafer 20 prior to planarization in accordance with the present invention having features that have a conformal layer of the material to be removed through planarization. The wafer portion 20 includes a substrate assembly 22 having a patterned dielectric layer 26 formed thereon. Such a patterned dielectric layer 26 can be used in a variety of structures, particularly a capacitor structure. The patterned dielectric layer 26 can be formed of any material that provides electrical isolation between metal regions (e.g., silicon dioxide, silicon nitride, or BPSG). An electrode layer 29 is then formed over the

substrate assembly 22 and the patterned dielectric layer 26. The electrode layer 29 may be platinum or any other suitable conductive second or third row Group VIIIB or Group IB metal-containing material. Generally, as shown in Figure 2A, the nonplanar upper surface 23 of electrode layer 29 is subjected to planarization or other processing in accordance with the present invention. The resulting wafer 20, as shown in Figure 2B, includes an upper surface 27 planarized such that the thickness of the wafer 20 is substantially uniform across the entire wafer 20 so that the wafer now includes electrically conducting regions 24 isolated within the patterned dielectric material 26 forming a capacitor structure. If desired, prior to planarization, the conformal layer 29 and openings 24 can be covered with a photoresist or other material that is removed after the planarization so the abrasive does not fall into the openings 24.